



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/507,357	09/10/2004	Patrik Jarl	P15400-US1	5702
27045	7590	09/28/2009		
ERICSSON INC. 6300 LEGACY DRIVE M/S EVR 1-C-11 PLANO, TX 75024			EXAMINER GORTAYO, DANGELINO N	
			ART UNIT	PAPER NUMBER
			2168	
			MAIL DATE	DELIVERY MODE
			09/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/507,357

Applicant(s)

JARL, PATRIK

Examiner

DANGELINO N. GORTAYO

Art Unit

2168

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 June 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SG/US)
- Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. In the amendment filed on 6/18/2009, Claim 16 has been amended. The currently pending claims considered below are Claims 13-24.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 13-24 are rejected under 35 U.S.C. 102(e) as being anticipated by

Paneth et al. (US Patent 6,393,002 B1)

As per claim 13, Paneth teaches “A processing unit (PA) for processing a plurality of data streams by an algorithm divided into a plurality of process steps,” (see Abstract and column 1 lines 33-58)

“said PA comprising: an interconnection unit comprising means for switching;”
(column 2 line 57 – column 3 line 4, Figure 2, column 8 lines 8-39, 57-67, column 9 lines 11-22, column 20 line 62 – column 25 line 13, wherein a channel control unit accepts streams from voice codec units and communicates with a remote-control processor unit in a base station to provide switching for a plurality of data streams)

"Process Step (PS) means comprising at least two PS modules, where each PS module is connected to the interconnection unit and a scheduler connected to said interconnection unit and to each PS module;" (Figure 5, column 25 line 5 – column 26 line 28, wherein modules are connected to a scheduler, a channel control unit, and the remote-control processing unit that is central to the system)

"a memory unit comprising at least two memories wherein each memory is connected to the interconnection unit;" (Figure 5, column 26 lines 7-28, column 47 lines 12-54, column 48 lines 19-57, wherein a database module contains memory connected to the modules and a channel control unit contains memory, both the module and the CCU are connected to the remote-control processor unit)

"the interconnection unit further comprising means for providing at least a first connection between one of said memories and one of said PS modules and a second connection between another of said memories and another of said PS modules, wherein the interconnection unit is adapted to connect each memory to each of the PS modules by a switching activity, wherein the switching activity and the processing of the PS modules are controlled by the scheduler;" (column 8 lines 25-67, column 25 line 5 – column 26 line 28, column 47 lines 13-58, wherein a remote-control processor unit is utilized to communicate between the CCU's and modules containing memory and scheduler for switching activity between a plurality of streams)

"and each memory comprises means for storing a data stream and said stored data streams are manipulated in parallel by the connected PS modules respectively, during a predetermined time period between said switching activities." (column 7 lines

24-59, column 26 lines 1-28, column 28 line 65 – column 29 line 60, column 35 lines 19-47, column 47 lines 12-58, wherein the database module and channel control units are utilized to store and transmit data streams according to the scheduler that can utilize timer events, as controlled by a remote-control processing unit)

As per claim 14, Paneth teaches “at least one external memory for storing at least input and output data for the memories within the memory unit.” (column 35 lines 50-64)

As per claim 15, Paneth teaches “said data streams are channels in a communication system.” (column 1 line 63 – column 2 line 9, column 6 lines 20-35, column 7 lines 15-30)

As per claim 16, Paneth teaches “said channels are speech channels and said PA is implemented in a speech coder.” (column 7 lines 15-30, column 43 lines 10-46)

As per claim 17, Paneth teaches “said process step modules are implemented by means of hardware suitable for the algorithm.” (column 8 lines 57-67, column 24 line 62 – column 25 line 5)

As per claim 18, Paneth teaches “at least one of the PS modules transfer data between the external memory and any of the memories within the memory unit.” (column 35 lines 19-47)

As per claim 19, Paneth teaches “A method for processing a plurality of data streams by an algorithm divided into a plurality of Process Steps (PS) by using an interconnection unit comprising means for switching,”

"Process Step (PS) means comprising at least two PS modules, each connected to the interconnection unit and a scheduler connected to said interconnection unit and to each PS module," (Figure 5, column 25 line 5 – column 26 line 28, wherein modules are connected to a scheduler, a channel control unit, and the remote-control processing unit that is central to the system)

"said method comprising the steps of: connecting at least two memories within a memory unit to the interconnection unit;" (Figure 5, column 26 lines 7-28, column 47 lines 12-54, column 48 lines 19-57, wherein a database module contains memory connected to the modules and a channel control unit contains memory, both the module and the CCU are connected to the remote-control processor unit)

"providing by the interconnection unit a first connection between one of said memories and one of said PS modules and a second connection between another of said memories and another of said PS modules, wherein the interconnection unit is adapted to connect each memory to each of the PS modules by a switching activity, wherein the switching activity and the processing of the PS modules are controlled by the scheduler;" (column 8 lines 25-67, column 25 line 5 – column 26 line 28, column 47 lines 13-58, wherein a remote-control processor unit is utilized to communicate between the CCU's and modules containing memory and scheduler for switching activity between a plurality of streams)

"storing a data stream in each memory," (Figure 5, column 26 lines 7-28, column 47 lines 12-54, column 48 lines 18-57, wherein a database module contains memory connected to the modules)

"and manipulating said data streams in parallel by the connected PS modules respectively, during a predetermined time period between said switching activities."
(column 7 lines 24-59, column 26 lines 1-28, column 28 line 65 – column 29 line 60, column 35 lines 19-47, column 47 lines 12-58, wherein the database module and channel control units are utilized to store and transmit data streams according to the scheduler that can utilize timer events, as controlled by a remote-control processing unit)

As per claim 20, Paneth teaches "storing at least input and output data for the memories within the memory unit at the at least one external memory." (column 35 lines 50-64)

As per claim 21, Paneth teaches "said data streams are channels in a communication system." (column 1 line 63 – column 2 line 9, column 6 lines 20-35, column 7 lines 15-30)

As per claim 22, Paneth teaches "said channels are speech channels and that said processing unit is implemented in a speech coder." (column 7 lines 15-30, column 43 lines 10-46)

As per claim 23, Paneth teaches "said process step modules are implemented by means of hardware suitable for the algorithm." (column 8 lines 57-67, column 24 line 62 – column 25 line 5)

As per claim 24, Paneth teaches "at least one of the PS modules transfers data between the external memory and any of the memories within the memory unit."
(column 35 lines 19-47)

Response to Arguments

4. Applicant's arguments, see page 5, filed 6/18/2009, with respect to the Objections to the Specification have been fully considered and are persuasive. The abstract filed 6/18/2009 has been accepted. The Objection of the Specification has been withdrawn.

5. Applicant's arguments, see page 5, filed 6/18/2009, with respect to the 35 USC 112, second paragraph rejection of claim 16 have been fully considered and are persuasive. The 35 USC 112, second paragraph rejection of claim 16 has been withdrawn.

6. Applicant's arguments, see page 5, filed 6/18/2009, with respect to the rejection of claims 13-24 in regards to 35 USC 102(e) have been fully considered but they are not persuasive.
 - a. Examiner is entitled to give claim limitations their broadest reasonable interpretation in light of the specification. See MPEP 2111 [R-I]

Interpretation of Claims-Broadest Reasonable Interpretation

During patent examination, the pending claims must be 'given the broadest reasonable interpretation consistent with the specification.' Applicant always has the opportunity to amend the claims during prosecution and broad

interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 162 USPQ 541,550-51 (CCPA 1969).

b. Applicant's arguments is stated as Paneth does not disclose "process modules coupled to an interconnection unit for selectively-coupled to different memory units under the control of a switching activity".

In regards to the argument, Examiner respectfully disagrees. As disclosed by Paneth in column 8 lines 58-67, a remote-control processor unit acts as a central control processor that connects the system of Paneth. The remote-control processor unit is connected to various application modules as described in column 25 line 5 - column 26 line 28, as well as to a channel control unit (CCU) containing memory. As disclosed by Paneth in the previously cited section, as well as specifically in column 35 lines 20-47, a database module contains the methods and interface for database access, which contains memory. In addition, column 47 lines 12-57 teaches that the CCU contains memory to store data stream information, both of which are in communication with the aforementioned central remote-control processor unit. The system also contains a scheduler module, described in column 28 line 65 – column 29 line 22 that controls scheduling of data processing tasks and data streams. As interpreted by the Examiner, the various process modules disclosed by Paneth are in communication with a central processor unit as well as both modules and system

parts containing memory to store data stream information, and therefore discloses "process modules coupled to an interconnection unit for selectively-coupled to different memory units under the control of a switching activity".

c. Applicant's arguments is stated as Paneth does not disclose "memory units that can each store a data stream and the stored data streams are manipulated in parallel by the connected process step modules, respectively, during a predetermined time period".

In regards to the argument, Examiner respectfully disagrees. As disclosed above, Paneth teaches database modules and a channel control unit that contains memory storage units to store data. In particular, column 47 line 12-54 and column 48 lines 18-57 teach that the CCU can contain memory information storing data stream information. The passage also discloses that data can be processed in parallel through the CCU and remote-control processing unit. The method to determine data processing schedule is executed by the scheduler module, disclosed in column 28 line 65 - column 29 line 22. As further disclosed in column 29 lines 23-60, the scheduler module can also determine when modules communicate with each other, and can make a scheduling system for parallel processing of data. As succinctly described in the Abstract of Paneth, digital information is received and sent in parallel over a system, and can be processed by the connected modules and processing units, through the central remote-control processing unit. Therefore, Paneth teaches "memory units that

can each store a data stream and the stored data streams are manipulated in parallel by the connected process step modules, respectively, during a predetermined time period".

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANGELINO N. GORTAYO whose telephone number is (571)272-7204. The examiner can normally be reached on M-F 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim T. Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dangelino N Gortayo/
Examiner, Art Unit 2168

Dangelino N. Gortayo
Examiner

/Tim T. Vo/
Supervisory Patent Examiner, Art
Unit 2168

Tim T. Vo
SPE